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U.S. UTILITY Patent Application

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APPLICANTS: Sasaki Chiyoshi; Hirata Kouji; Itoh Katsushi; Ootori Yasuhiro; Kubota Ryoutichi;					
CONTINUING DATA VERIFIED:					
FOREIGN APPLICATIONS VERIFIED: JAPAN 2000-325092 10/25/2000					
DO NOT PUBLISH <input type="checkbox"/> RESCIND <input type="checkbox"/>					
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no			ATTORNEY DOCKET NO		
35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no			100809-00050(SCET 19.098)		
Verified and Acknowledged Examiners's initials					
TITLE : Circuit substrate unit and electronic equipment					

U.S. DEPT. OF COMM/PAT & TM-PTO-436L(Rev. 12-94)

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NOTICE OF ALLOWANCE MAILED 7/21/03		Assistant Examiner	CLAIMS ALLOWED Total Claims 22 Print Claim for O.G. 3(1)	
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<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner PREPARED FOR ISSUE	Application Examiner Kenji Duncan 7/23/03	
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